## REMARKS

Claims 1, 5-10, 26, 27, 29, and 32-33 remain in the application. Claims 2-4, 11-25, 28, and 30-31 have been cancelled.

By this amendment, applicants have amended claims 1, 26, and 29 to more particularly point out and distinctly claim the subject matter that applicants regard as their invention. FIGS. 4 and 6 and/or paragraph [0027] in the specification support the changes to claims 1 and 26. FIG. 4 supports the change to claim 29.

Also, claim 10 has been amended to correct a grammatical error.

## Submission of Present Amendment is respectfully requested

Pursuant to 37 C.F.R. 1.116(b)(2) & (3), applicants believe that this amendment places their application in better form for allowance or consideration on appeal. Moreover, applicants respectfully believe that this amendment touches on the merits of their application, and they did not present the amendments and remarks made herein until now because new grounds for rejection were first raised in the present Office Action to which this amendment is responsive to.

Applicants therefore respectfully request that Examiner Nadav grant the admission of the present amendment under 37 C.F.R. 1.116(b)(2) & (3).

TO:USPTO

## Response to 35 U.S.C. §112 Rejection

Claims 1-10 and 26-33 were rejected under 35 U.S.C. §112, first paragraph for failing to comply with the written description. Claims 2-4, 28, and 30-31 have been cancelled by this amendment making the rejection of these claims now moot. Applicants have amended claims 1 and 26 to both call for an intermediary semiconductor structure and to eliminate the substantially filled language. Thus, applicants respectfully believe that claims 1, 5-10, 26, 27, 29, and 32-33 meet the requirements of §112, first paragraph.

## Response to 35 U.S.C. §103(a) Rejection

Claims 1-10 and 26-33 were rejected under 35 U.S.C. §103(a) as being unpatentable over Lur et al. USP 5,640,041, ("Lur") in view of Davies, USP 6,512,283 ("Davies"). Claims 2-4, 28, and 30-31 and have been cancelled by this amendment making the §103 rejection of these claims moot. The rejection on the balance of the claims is respectfully traversed in view the amendments made herein and the remarks made hereinafter.

Claim 1 has been amended to call for an intermediary semiconductor device comprising a semiconductor substrate having a surface formed with a first recessed region. A first dielectric material is formed in the first recessed region. A second recessed region is formed within the first dielectric material, wherein the second recessed region has walls, a lower surface, and a first opening in

TO:USPTO

proximity to the surface. A semiconductor layer is formed overlying the first dielectric material and has a second opening at least partially over the first opening, wherein at least a portion of the semiconductor layer is configured to convert to a semiconductor oxide that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is exposed to an oxidizing environment.

Applicants respectfully submit that the combination of Lur and Davies fails to make claim 1 obvious for at least the following reasons. Specifically, neither reference either singularly or in combination shows or suggests a semiconductor layer formed overlying the first dielectric material and has a second opening at least partially over the first opening, wherein at least a portion of the semiconductor layer is configured to convert to a semiconductor oxide that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is exposed to an oxidizing environment. More specifically, Lur's layer 5 has no opening at all, and Davies is completely silent on this element. Further Lur does not show or suggest that layer 5 is configured to convert to a semiconductor oxide that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is exposed to an oxidizing environment.

Claims 5-10 depend from claim 1 and are believed allowable for at least the same reasons as claim 1.

Claim 26 calls for an intermediary of a semiconductor device comprising a semiconductor substrate having a

TO: USPTO

surface formed with a first recessed region. A first dielectric material is deposited in the first recessed region and is formed with a second recessed region having a first opening and walls. A semiconductor cap layer is formed overlying the first dielectric material and has a second opening at least partially over the first opening, wherein at least a portion of the semiconductor cap layer is configured to convert to a semiconductor oxide that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is exposed to an oxidizing environment.

Applicants respectfully submit that the combination of Lur and Davies fails to make claim 26 obvious for at least the following reasons. Specifically, neither reference either singularly or in combination shows or suggests a semiconductor layer formed overlying the first dielectric material and has a second opening at least partially over the first opening, wherein at least a portion of the semiconductor layer is configured to convert to a semiconductor oxide that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is exposed to an oxidizing environment. More specifically, Lur's layer 5 has no opening at all, and Davies is completely silent on this element. Further Lur does not show or suggest that layer 5 is configured to convert to a semiconductor oxide that covers the first opening while leaving a void in the second recessed region when the semiconductor substrate is exposed to an oxidizing environment.

P.10/10

ONS00317 10/072,145

Claims 27, 29, and 32-33 depend from claim 26 and are believed allowable for at least the same reasons as claim 26.

6022443169

In view of the above, it is believed that the claims are allowable, and the case is now in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

Attorney for Applicant(s)

Guy E. Averett et al.

Kevin B. Jackson

Reg. No. 38,502

Tel. (602) 244-5306

ON Semiconductor Law Dept./MD A700 P.O. Box 62890 Phoenix, AZ 85082-2890

Date: April 13, 2006